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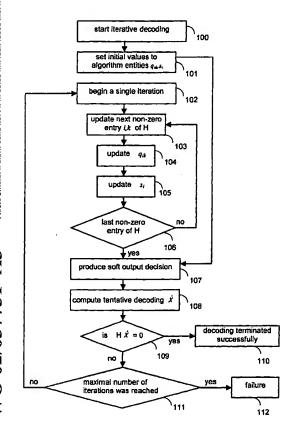
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[Continued on next page]

(54) Title: DECODING OF LOW DENSITY PARITY CHECK CODES



(57) Abstract: A method of decoding a data signal using a low density parity check matrix, comprising a first stage of iteratively carrying out horizontal and vertical decoding steps to form a matrix (102) and a second stage of testing for parity (109), characterized in that the elements of the matrix are updated sequentially (104), such that each element of the matrix is employable for subsequent calculations as soon as it is updated.

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A. CLASSIFICATION OF SUBJECT MATTER  IPC(7) : H 03 M 13/00  US CL : 714/752  According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED				
Minimum documentation searched (classification system followed by classification symbols) U.S.: 714/752, 714/746, 714/for.102				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) IEEE database - Gallager, LDPC, matrix update, efficient decoder, parity matrix				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category *	Citation of document, with indication, where appropriate, of the relevant passages			Relevant to claim No.
Α	MacKay, D.J.C. and Neal. R.M. Near Shannon limit performance of low density parity			1-14
Y	check codes IEEE, Electronic Letters, 29 August 1996, Vol. 32 No. 18, pages 1645-1646, especially page 1646.			15-20
A	US 4,295,218 A (Tanner) 13 October 1981 (13.10.1978), column 15, lines 34-68, column 16, lines 1-42.			1-14
Y	US 5,515,387 A (Smith) 07 May 1996 (07.05.1996), column 5, lines 8-44.			15-20
Further	documents are listed in the continuation of Box C.	See pater	nt family annex.	
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